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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,972	06/29/2001	Yngve Ternulf	0104-0345P	5129

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
YANG, RYAN R	

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/856,972	TERNULF ET AL.	
	Examiner	Art Unit	
	Ryan R. Yang	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2005* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1/ A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/11/2005 has been entered.

2. This action is responsive to communications: Amendment, filed on 2/11/2005. This action is non-final.

3. Claims 1-21 are pending in this application. Claims 1 and 12 are independent claims. In the Amendment, filed on 2/11/2005, claims 1 and 12 were amended.

4. This application is a 371 of PCT/SE98/02183 filed 11/30/1998.

5. The present title of the invention is "Method for inserting objects into a working area in a computer application" as filed originally.

Claim Rejections - 35 USC § 102

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1-5, 7, 9-16, 18 and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Katoh et al. (6,173,433).

8. As per claim 1, Kato et al., hereinafter Kato, discloses a method for creating a logical network by inserting a plurality of objects into a working area on a computer display, comprising the step of:

Displaying an existing network in said working area (Figure 8- 107 "The operator lays out and designs an optical circuit by displaying a layout drawing on the display screen of the display 107", column 12, line 33-35);

identifying at least one subarea of the working area where an object is validly insertable into said network ("to enable a virtual path to be generated, connection terminals for two associated blocks are provided by the operator specifying them", column 17, line 33- line 35, where the path between the terminals is considered a subarea);

identifying at least one type of object that can be validly inserted into the network in said subarea ("when the positions and directions of the connection terminals of two parts are indicated, a path for the waveguide that is to be installed between the two connection terminals, that is a propagation path for optical waves or microwaves is automatically determined", column 4, line 54-56);

visually indicating said at least one subarea (Figure 3A-3D where 4 virtual path is indicated);

visually Indicating said at least one object type in association with each indicated subarea (Figure 22 "the circuit design system generates a plurality of possible paths as candidates for the propagation path when the positions and directions of two points are given", column 4, line 35-38; and

receiving input from the user selecting one of said at least one object type indicated in association with one of said at least one subarea ("when the operator uses mouse to operate a determination button 705 on the display screen, the CPU 101 finishes a standard circuit part election process", column 16, line 22-24),

displaying an extended network where an additional object of the selected type is inserted into the selected subarea ("Finally, the CPU 101 regenerates the path connected to the blocks obtained after the movement and displays it on the display 107", column 28, 24-26), and

said steps being performed by a computer application software for creating a logical network (Figure 8 depict a optical circuit design system incorporating image processing software, column 11, line 31-35; the optical circuit is considered a network and the image processing software is considered an application software).

9. As per claim 2, Kato demonstrated all the elements as applied to the rejection of independent claim 1, supra, and further discloses the step of identifying at least one subarea of the working area where an object is insertable into said network comprises the step of graphically outlining said at least one subarea (Figure 3A – 3D).

10. As per claim 3, Kato demonstrated all the elements as applied to the rejection of claims 1 or 2, supra, and further discloses the identification of said at least one subarea is activatable and deactivatable by the user ("The block layout submenu item 611 instructs a target block to be generated. When the operator uses that mouse to select the submenu item 611, the CPU 101 generates a block according to the processing procedure of the image processing program shown in Fig. 28. The CPU 101 first

recognizes from the position indicated by the mouse that the block layout procedure has been indicated", column 15, line 56-62, thus, indicating the selected area is activated).

11. As per claim 4, Kato demonstrated all the elements as applied to the rejection of independent claim 1, supra, and further discloses wherein input from the user is received using a pointing device (Figure 8-108 where the input device can be a mouse or keyboard, column 11, line 40).

12. As per claim 5, Kato demonstrated all the elements as applied to the rejection of dependent claim 4, supra, and further discloses the pointing device is in electronic contact with the computer application and controls a cursor on the display ("Another method isto move the mouse cursor to the block graphics to be grouped ", column 14, line 25-27, thus, indicating the pointing device is in electronic contact with the computer application and controls a cursor).

13. As per claim 7, Kato demonstrated all the elements as applied to the rejection of dependent claim 4, supra, and further discloses the step of indicating an object type in association with each subarea comprises the step of displaying a symbol representing said object type in connection to said subarea (Figure 22).

14. As per claim 9, Kato demonstrated all the elements as applied to the rejection of independent claim 1, supra, and further discloses the object types represent various physical items that are inserted into the working area to create said network (Figure 22 shows different types of circuit).

15. As per claim 10, Kato demonstrated all the elements as applied to the rejection of dependent claim 9 supra, and further discloses the network represents a system for

automation ("the CPU then references the rule of virtual path generation to automatically generate a virtual path connecting the connection terminals of the two blocks", Abstract)

16. As per claim 11, Kato demonstrated all the elements as applied to the rejection of independent claim 1 supra, and further discloses computer-readable medium, on which is stored instructions for one or several general purpose computers, comprising means for enabling said one or said several computers to perform the steps of the method according to claim 1 (Since the invention by Kato is a computer program useful in a computer system, it is inherent the program is stored in a computer-readable medium to be executed on a computer).

Claim Rejections - 35 USC § 103

17. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al., and further in view of Cariffe et al. (6,201,548).

As per claim 6, Kato demonstrated all the elements as applied to the rejection of dependent claim 4 or 5, supra.

Kato discloses a method for inserting an object into a working area. It is noted that Kato and Wright do not explicitly disclose the step of identifying at least one subarea of the working area where an object is insertable into said network comprises the step of graphically outlining said subarea when the cursor is moved into said subarea, however, this is known in the art as taught by Cariffe et al., hereinafter Cariffe.

Cariffe discloses an image editing method in which a portion of the image is outlined when the cursor is moved into the subarea (column 1, line 16-18).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Cariffe into Kato because Kato discloses a method for inserting an object into a working area and Cariffe discloses the area of interest the cursor moves into is outlined in order for it to be easily distinguished from the rest of the area.

18. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al., and further in view of Hernandez et al. (4,686,522).

As per claim 8, Kato demonstrated all the elements as applied to the rejection of dependent claim 5, supra.

Kato discloses a method for inserting an object into a working area. It is noted that Kato does not explicitly disclose the step of indicating an object type in association with each subarea comprises the step of changing the appearance of the cursor, however, this is known in the art as taught by Hernandez et al., hereinafter Hernandez. Hernandez discloses a method of editing graphics objects in which the appearance of the cursor changes when associated with a region ("while only one cursor is displayed, its appearance is changed from a blinking cursor to a pointing cursor during the process which is selecting the particular action", column 2, line 51-54).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Hernandez into Kato because Kato discloses a method for inserting an object into a working area and Hernandez discloses

appearance of the cursor changes when associated with a region in order to easily edit a graphical object.

19. As per claims 12-21, since they are directed to an apparatus for performing the method of claims 1-10, and therefore are similarly rejected as claims 1-10, respectively.

Regarding the "means plus function" language, the means refer to the software methods executed on generically disclosed hardware explicitly disclosed by Kato, Cariffe and Hernandez. It is further noted that both software and hardware means are functionally equivalent.

Response to Arguments

20. Applicant's arguments filed 2/11/2005 have been fully considered but they are not persuasive.

Applicant alleges Katoh does not teach displaying subareas where an object is validly insertable. In reply, examiner considers by identifying two terminals, a subarea is also identified- "to enable a virtual path to be generated, connection terminals for two associated blocks are provided by the operator specifying them", column 17, line 33-line 35, where the path between the terminals is considered a subarea. Since only area between terminals can have valid path, only these area can accept an object.

Applicant alleges Katoh's invention is not concerned with a logical network. In reply, examiner considers Katoh's circuit can perform as a logical network.

Applicant also alleges Katoh does not teach the steps being performed by a computer applicant software. In reply, examiner considers Figure 8 depicts a computer system using application software to perform claimed invention.

Inquiries

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan R Yang whose telephone number is (571) 272-7666. The examiner can normally be reached on M-F 9:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Yang
August 7, 2005